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L3: Entry 2 of 3 File: USPT Apr 23, 2002

DOCUMENT-IDENTIFIER: US 6376341 B1
TITLE: Optimization of thermal cycle for the formation of pocket implants

Brief Summary Text (14):
In one form, a process for fabricating a memory cell includes providing a semiconductor substrate and forming an ONO layer over the semiconductor substrate. A masking layer, such as silicon nitride or polysilicon, is then deposited overlying the ONO layer and patterned into a resist mask. The resist mask is thick enough to withstand both an n-type and a p-type implant and go through an annealing process. After patterning the masking layer into a resist mask, the semiconductor substrate is doped with p-type dopants such as boron, preferably by using ion implantation. The p-type implant is a direct implant, which is an implant at an angle substantially normal with respect to the principal surface of the semiconductor surface. The p-type implant creates a p-type region. After performing the p-type implant, the semiconductor substrate is then exposed to a thermal cycle to laterally diffuse the p-type region to the desired regions of the semiconductor substrate. After exposing the semiconductor substrate to a thermal cycle, the semiconductor substrate is then doped with an n-type dopant such as arsenic, preferably by using ion implantation. The doping of the semiconductor substrate with an n-type dopant causes an n-type region to form in the semiconductor substrate. Preferably, the n-type implant is a direct implant. In one preferred embodiment, an etch is applied to the exposed ONO layer to expose part of the semiconductor substrate before the doping of the semiconductor substrate with an n-type dopant. After doping the semiconductor substrate with an n-type dopant, the resist mask is removed and the bit-line oxide region is formed.

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L3: Entry 2 of 3 File: USPT Apr 23, 2002

US-PAT-NO: 6376341
DOCUMENT-IDENTIFIER: US 6376341 B1

TITLE: Optimization of thermal cycle for the formation of pocket implants

DATE-ISSUED: April 23, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kluth; George J.	Sunnyvale	CA		
Halliyal; Arvind	Sunnyvale	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 09/ 627584 [PALM]
DATE FILED: July 28, 2000

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATION This application claims the benefit under 35 U.S.C. .sctn. 119(e) of the U.S. provisional application Ser. No. 60/210,397, filed on June 9, 2000.

INT-CL: [07] H01 L 21/04

US-CL-ISSUED: 438/510; 438/257, 438/258, 438/266
US-CL-CURRENT: 438/510; 257/E21.21, 438/257, 438/258, 438/266

FIELD-OF-SEARCH: 438/510, 438/258, 438/257, 438/216, 438/769, 438/266

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5409848	April 1995	Han et al.	
☐	5933729	August 1999	Chan	

ART-UNIT: 2823

PRIMARY-EXAMINER: Picardat; Kevin M.

ASSISTANT-EXAMINER: Collins; D. M.

ATTY-AGENT-FIRM: Amin & Turocy, LLP

ABSTRACT:

A process for fabricating a memory cell, the process includes forming an ONO layer overlying a semiconductor substrate, depositing a masking layer overlying the ONO layer, patterning the masking layer into a resist mask, implanting the semiconductor substrate with a p-type dopant to create a p-type region, and laterally diffusing the p-type region. In one preferred embodiment, the lateral diffusing of the p-type region includes exposing the semiconductor substrate to a thermal cycle. Preferably, the thermal cycle is a rapid thermal anneal or a furnace anneal.

20 Claims, 6 Drawing figures

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L4: Entry 8 of 15 File: USPT Oct 29, 2002

DOCUMENT-IDENTIFIER: US 6472701 B2
TITLE: Non-volatile semiconductor memory device and its manufacturing method

Detailed Description Text (23):
Thereafter, a resist layer 9 is coated and patterned as shown in FIGS. 7A-7C. The SiN film 8 is etched by anisotropic etching (in the memory cell section), and then the resist layer is removed. Referring then to FIGS. 8A-8C, the control gate layer (polysilicon layer) 7 and then the ONO film 6 are etched by anisotropic etching, using the SiN film 8 as a mask. At this time, the memory cell section has a structure as shown in FIG. 8A in which the films 8-6 are treated for the formation of a gate electrode, while the peripheral sections have structures as shown in FIGS. 8B and 8C, in which the floating gate layer is exposed.

Detailed Description Text (39):
Then, as in the second embodiment, the SiN film 8 is used as a mask to etch the control gate layer and the ONO film by anisotropic etching, and the resist is removed. In the following steps which are not shown, resist is coated and patterned, and then the floating gate layer is etched by anisotropic etching, using, as masks, those portions of the resist provided on the gate electrodes of the peripheral transistors and on the contact portion of the resistive element, and those portions of SiN provided in the memory cell section and on the other portion of the resistive element. Then, the resist is removed.

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L4: Entry 8 of 15 File: USPT Oct 29, 2002

US-PAT-NO: 6472701
DOCUMENT-IDENTIFIER: US 6472701 B2

TITLE: Non-volatile semiconductor memory device and its manufacturing method

DATE-ISSUED: October 29, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yaegashi; Toshitake	Yokohama			JP
Shimizu; Kazuhiro	Yokohama			JP
Aritome; Seiichi	Yokohama			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Kabushiki Kaisha Toshiba	Tokyo			JP	03

APPL-NO: 09/ 741261 [PALM]
DATE FILED: December 19, 2000

PARENT-CASE:
This is a division of application Ser. No. 09/112,482, filed Jul. 9, 1998, now U.S. Pat. No. 6,265,739, which application is hereby incorporated by reference in its entirety.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	9-184863	July 10, 1997

INT-CL: [07] H01 L 27/108

US-CL-ISSUED: 257/296; 257/908
US-CL-CURRENT: 257/296; 257/908

FIELD-OF-SEARCH: 257/296, 257/392, 257/908

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5600164	February 1997	Ajika et al.	257/321
☐	5824583	October 1998	Asano et al.	438/258
☐	5841174	November 1998	Arai	257/392
☐	5852311	December 1998	Kwon et al.	257/315
☐	5913120	June 1999	Cappelletti	438/257

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
2-246376	October 1990	JP	257/320
5-183134	July 1993	JP	438/396
5-190811	July 1993	JP	
8-23041	January 1996	JP	

OTHER PUBLICATIONS

Wolf et al. "Silicon Processing for the VLSI Era," 1986, Lattice Press, vol. 1, pp. 384-388.

ART-UNIT: 2815

PRIMARY-EXAMINER: Wilson; Allan R.

ATTY-AGENT-FIRM: Hogan & Hartson, LLP

ABSTRACT:

In a non-volatile semiconductor memory device and a method for manufacturing the device, each memory cell and its select Tr have the same gate insulating film as a Vcc Tr. Further, the gate electrodes of a Vpp Tr and Vcc Tr are realized by the use of a first polysilicon layer. A material such as salicide or a metal, which differs from second polysilicon (which forms a control gate layer), may be provided on the first polysilicon layer. With the above features, a non-volatile semiconductor memory device can be manufactured by reduced steps and be operated at high speed in a reliable manner.

2 Claims, 84 Drawing figures

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L4: Entry 9 of 15 File: USPT Aug 13, 2002

DOCUMENT-IDENTIFIER: US 6433384 B1
TITLE: Semiconductor memory device having sources connected to source lines

Detailed Description Text (18):
Thereby, the word line WL connected to the control gates of the semiconductor memory cells MC is thus formed. After that, a stacked gate electrode is formed by using the silicon nitride oxide film 111 as a mask to etch the ONO film 107 and the polysilicon film 106.

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L4: Entry 9 of 15 File: USPT Aug 13, 2002

US-PAT-NO: 6433384
DOCUMENT-IDENTIFIER: US 6433384 B1

TITLE: Semiconductor memory device having sources connected to source lines

DATE-ISSUED: August 13, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hashimoto; Hiroshi	Kawasaki			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Fujitsu Limited	Kawasaki			JP	03

APPL-NO: 09/ 627457 [PALM]
DATE FILED: July 27, 2000

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	11-215601	July 29, 1999

INT-CL: [07] H01 L 29/788

US-CL-ISSUED: 257/316; 257/347, 257/763
US-CL-CURRENT: 257/316; 257/347, 257/763

FIELD-OF-SEARCH: 257/315, 257/316, 257/321, 257/347, 257/754, 257/763

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5270240	December 1993	Lee	257/321
☐	6044016	March 2000	Itoh	257/316
☐	6069383	May 2000	Yu	257/316

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
5-145047	June 1993	JP	
8-106791	April 1996	JP	
9-275197	October 1997	JP	
2833030	October 1998	JP	

ART-UNIT: 2813

PRIMARY-EXAMINER: Chaudhari; Chandra

ATTY-AGENT-FIRM: Armstrong, Westerman & Hattori, LLP

ABSTRACT:

A semiconductor memory device includes a silicon semiconductor substrate, a plurality of element isolation regions formed on the silicon semiconductor substrate, a plurality of semiconductor memory cells formed between the element isolation regions, and conductive films formed on the silicon semiconductor substrate and connecting to source diffusion regions of at least two of the semiconductor memory cells.

12 Claims, 31 Drawing figures